

ABSTRACT

A structure is disclosed for split-gate flash memory cells in which isolation regions separate parallel active regions within a semiconductor region. Trapezoidal floating gates, separated from the active regions by an insulator layer, are equally spaced over the active regions. Three tiered parallel strips run perpendicular to the active regions and pass over corresponding trapezoidal floating gates, the bottom and top tiers being insulator layers and the middle tier being a conductor layer. Insulator spacers are disposed over the sidewalls of the three-tiered parallel strips and of the trapezoidal floating gates. These parallel structures are designated floating gate towers. Source/drain regions are formed in the semiconductor region of every other opening between floating gate towers where they are contacted by source/drain contact lines. An insulator layer is disposed over the source/drain contact lines. The other openings between floating gate towers contain select gates, which are conductive columns that are separated from the semiconductor region by an insulator layer and rise over active regions. Parallel select gate contact lines are disposed over and run along the active regions contacting the select gates.